

Data Sheet

VIAVI

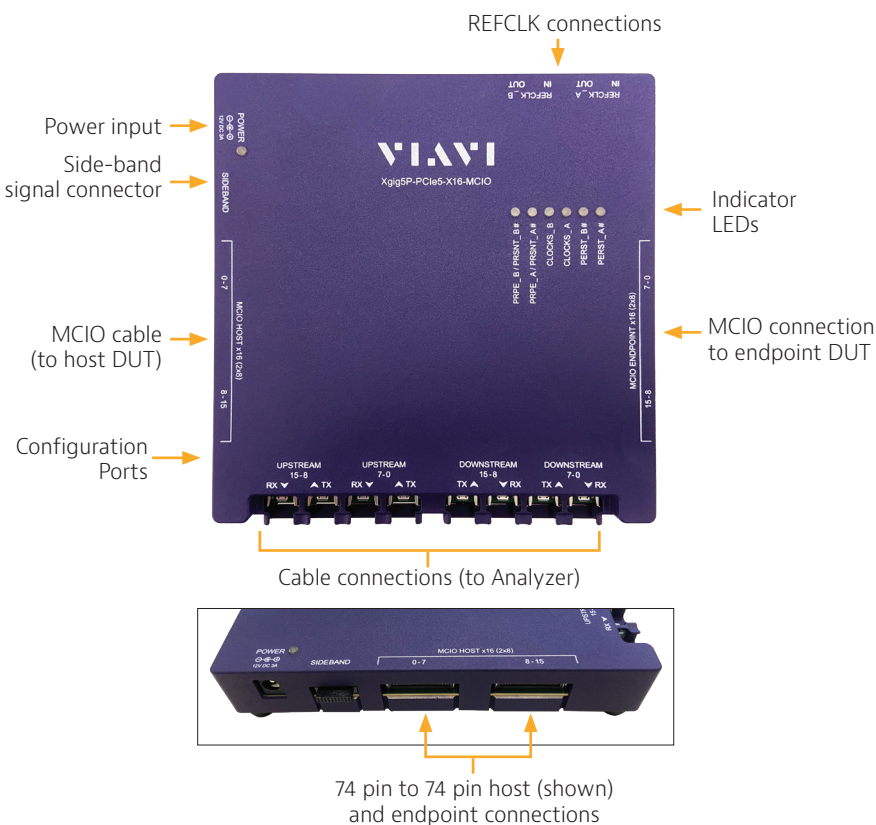
Xgig MCIO 16-lane Interposer

for PCI Express® 5.0

Provides a tap of MCIO/CopprLink™ PCIe signals for input to the VIAVI PCIe 5.0 Analyzer

VIAVI Solutions Xgig® MCIO Interposer, the Xgig5P-PCIe5-X16-MCIO, supports analysis of PCIe5 communication across an MCIO/CopprLink internal connection. This Interposer enables protocol analysis of communication between a 16-lane MCIO host port and an MCIO attached endpoint device. Bidirectional PCIe 5.0 protocol data on each of 16 lanes is captured at up to 32GTps rate for analysis. High-performance, low-loss, custom cables are supplied for connection into the VIAVI Analyzer.

This Interposer uses high-speed linear signal redrivers to buffer the system data signals ensuring a clean signal is delivered to both the Analyzer and the devices-under-test



Key Features

- Operates at 32GT/s PCIe 5.0 data rates, and is compatible with PCIe rates of 2.5, 5.0, 8.0 and 16GT/s
- Two, 74 pin to 74 pin MCIO connectors on each side of the interposer pod support PCIe links of up to 16-lanes
- Supplied with high-quality custom cables for Analyzer attachment
- Data path uses high-speed linear redrivers to ensure good signal capture with minimal tuning
- Supports Analyzer side-band signal capture and triggering via custom cable
- Cables supplied for optional clocking sources
- Interposer power is independent of host system
- A 120/220 AC in, 12V/3A DC output converter is included
- LEDs give quick indication of power and operation
- Size: (L x W x H): 165 x 156 x 27 mm (excl. rubber stands)
- Works with multiple VIAVI Xgig 5P Analyzer types
- Provides consistent, repeatable capture of link training, equalization negotiation and other data
- Supports Jammer error injection for deep system analysis and debug
- Up to two Interposers are stackable to support wider length widths
- Supported by VIAVI Xgig tool suite including Trace Control, Expert™ and Serialytics™

Applications

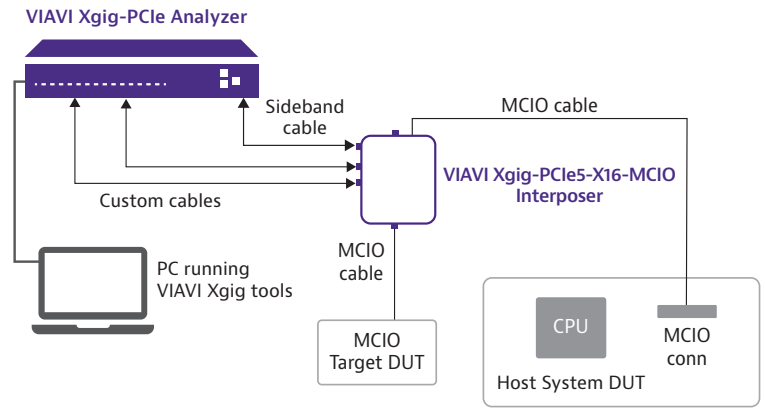
Working together with the VIAVI PCIe 5.0 Analyzer/ Exerciser/Jammer platform, the Interposer enables debug and validation of new ICs with MCIO interface, MCIO peripherals, host system implementations, firmware and drivers, validation of system BIOS and software, error injection, and for manufacturing test. It supports full decode and analysis of PCIe data traffic and link states.

To install the Xgig5P-PCIe5-X16-MCIO Interposer, with the system power-off, connect the Interposer into the MCIO cable path and to the Analyzer chassis using the supplied MCIO/CopprLink internal cables. Power-on the Interposer and Analyzer, specify the trace capture conditions using the Xgig tools and then power-up the system under test.

The block diagram to the right indicates the signal data path. Data flows between the host system’s MCIO interface and the MCIO target DUT as normal. The signal is “tapped” for use by the Analyzer inside the Interposer.

When operating in Analyzer mode, the DUT data is captured (tapped) from both the upstream and downstream data paths as inputs to the Analyzer. When operating in Jammer mode, or Analyzer/Jammer mode, data flows through the Analyzer chassis.

In addition to this 16-lane MCIO Interposer, VIAVI offers a variety of other Interposer types for connecting into many popular PCIe system applications, including CEM, U.2, M.2, EDSFF, CDFP, OCP3 Flying-Lead and others.



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Kit Contents

Item	Description	Qty
1	X16-MCIO Interposer pod for PCIe 5.0	1
2	74p to 74p MCIO (aka CopprLink™) internal cables	4
3	Custom high-performance cables	2
4	Sideband signal cable (to Analyzer)	1
5	MCX 50-Ohm coax cables for optional clock	2
6	Power brick, 120/220 input, 12V/3A output	1
7	Quick Start Guide	1

Ordering Information

Part Number	Description
Xgig5P-PCIe5-X16-MCIO	MCIO Interposer, 16-lane, 32GTps, for PCIe 5.0
XGIG-INTPSR-C-Hx (x=1, 2, 3, 4)	x-year extended hardware warranty



Contact Us **+1 844 GO VIAVI**
(+1 844 468 4284)

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visit viasolutions.com/contact

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