

# Bamboozled by Bit Errors?

Conventional test equipment can count bit errors – but often lacks the deep insights necessary to identify design flaws and product performance problems.

Modern high-speed links for the fastest Ethernet rates of 400GbE and above use [PAM-4](#) electrical modulation. This modulation format allows interfaces to run at the speeds required for 400GbE and above, but PAM-4 modulation is more susceptible to the impacts of noise and signal integrity.

This is mitigated by the use of forward error correction (FEC) coding, which is integrated into the Ethernet stack. Even with FEC, it is critical to understand all the errors in a link as some may be indications of marginal product performance or even a significant design flaw.

Conventional test equipment can count bit errors, but this gives no insight into the nature of the errors. Engineers are blindly troubleshooting and laboring to understand the real issues and may even completely miss a fundamental design flaw. VIAVI has developed comprehensive and integrated tool sets that give clear indication into magnitude of the errors and deep insight into their nature to help resolve things more quickly.

## Which BERT at each part of the product development timeline?

As a product evolves through its development lifecycle it is important to get the optimal feature match to the needs so product development stays on track.

The following table helps highlight the needs through the development lifecycle:

Lifecycle Stage	Key Requirements	Product Fit
Silicon development and validation	<ul style="list-style-type: none"> <li>High parametric accuracy and control over TX</li> <li>Waveform mask, jitter injection and analysis</li> </ul>	<ul style="list-style-type: none"> <li>AWG + real time oscilloscope.</li> <li>Parametric BERT</li> <li>VIAVI ONT IP validation and development</li> </ul>
Product development	<ul style="list-style-type: none"> <li>Support for module form factor</li> <li>Unframed and framed/Ethernet traffic</li> <li>Error analysis</li> </ul>	<ul style="list-style-type: none"> <li>VIAVI ONT                             <ul style="list-style-type: none"> <li>includes support for traffic and module management</li> </ul> </li> </ul>
Product validation and vendor selection	<ul style="list-style-type: none"> <li>Support for module form factor</li> <li>Unframed and framed/Ethernet traffic</li> <li>Error analysis.</li> <li>Clear and concise pass/fail</li> <li>Automation support</li> </ul>	<ul style="list-style-type: none"> <li>VIAVI ONT                             <ul style="list-style-type: none"> <li>includes support for traffic and module management</li> </ul> </li> </ul>
Production test	<ul style="list-style-type: none"> <li>Low cost, high throughput</li> </ul>	<ul style="list-style-type: none"> <li>Low cost BERTs per test stand backed by VIAVI ONT based 'Golden' test station</li> </ul>

Parametric BERT, AWG and real time oscilloscopes are ideal for the silicon validation stage, but they are not effective for the other stages of the product development lifecycle. They lack the native form factor support, framed traffic and deeper analysis needed for product development, validation, vendor selection and production. In the past, engineers may have turned to a simple unframed BER, but with the advent of PAM-4 deeper analysis is required.

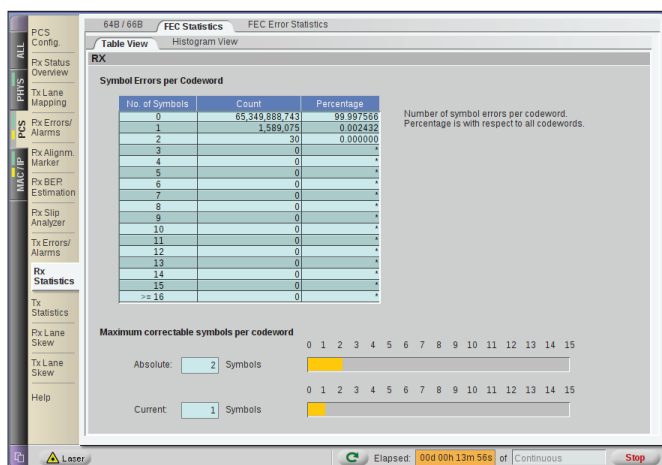
In the next section we examine why basic BER no longer is useful.

## Why BER Doesn't Help

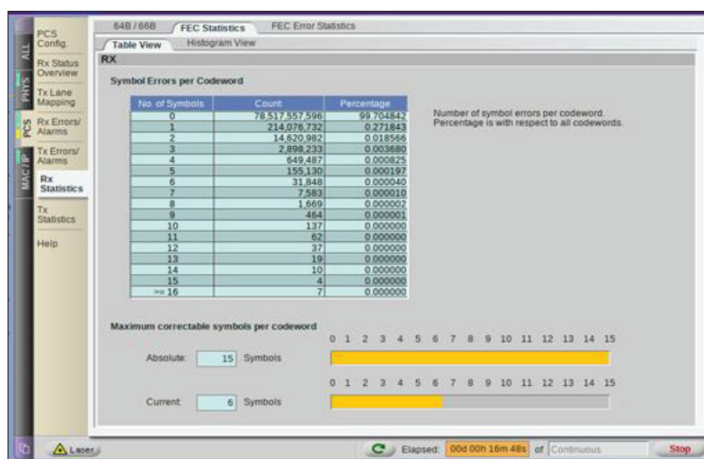
Bit error rate is a coarse measurement – it basically tells you how many bits are in error over a time interval. Even with fine time granularity, you can still be looking at billions of bits, and the basic bit error rate (BER) doesn't help in understanding how the errors are distributed and if they actually are a cause for concern.

The first place to start is looking at the FEC errored symbols per codeword profile.

The two examples below were generated on equipment, that when tested with a conventional BER tester, gave very similar results. But when examined using the VIAVI ONT-800 FEC errored symbols view, a very different picture emerges.



Case 1: A 'good' FEC tail with rapid fall-off of errored symbols per code word



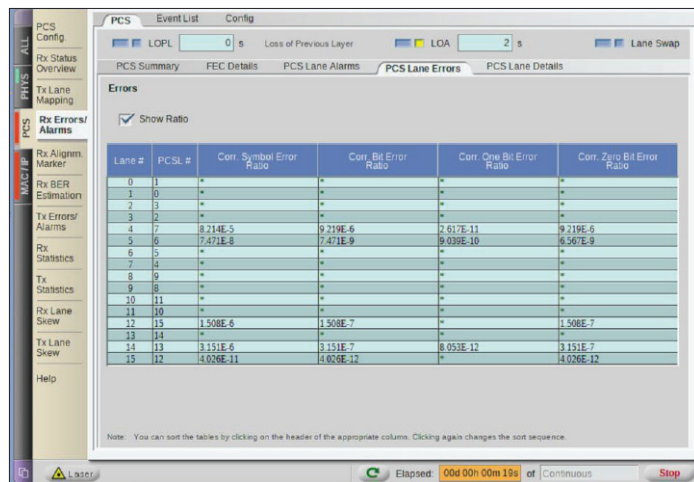
Case 2: A 'bad' FEC tail with a long tail leading to uncorrectable code words and dropped packets

Both the above images occur at approximately the same BER, a simple BERT would not show any significant difference between the two cases so a simple pass/fail threshold would allow bad parts to be used!

The VIAVI errored symbols per codeword view gives critical information at a glance. The length and shape of the tail can quickly give the experienced engineer a lot of information. A short tail with a rapid monotonic fall off to zero errored symbols above the 5 counts (after a reasonable run time) is a result which would give no major concern, but extended and non-monotonic tails must be investigated further.

The next stage is to understand why there are so many errored symbols in Case 2.

The [VIAVI ONT family](#) offers a lot of unique tools to dig into this. The ONT can track the error profile and detect error bursts and bit slips – a potential cause of ‘bad’ FEC tails.



VIAVI ONT-800 bit slip view

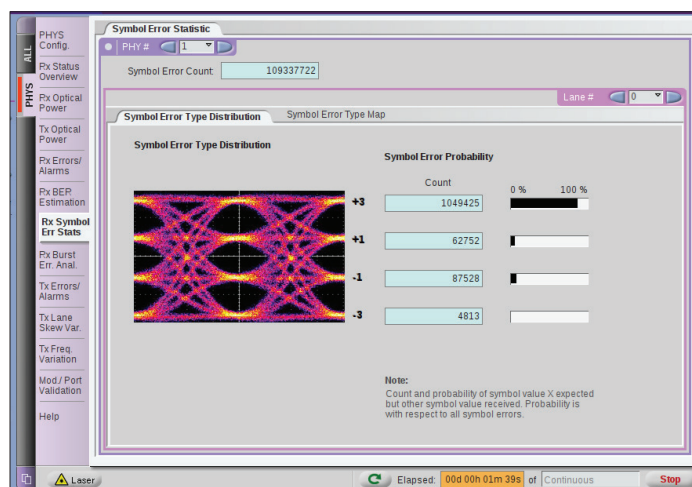
The Rx Slip analysis view quickly identifies issues with several of the logical lanes having significant bit slips. This would cause the bad FEC tail we see in Case 2.

The designer can then make appropriate changes (this could include altering TX equalizer settings and updating DSP firmware).

To further ensure design robustness, the user can stress the link with the ONT [Dynamic Skew](#) feature – this maximizes the chance of crosstalk and also stresses modern DSP based CDRs and equalizers to ensure they have enough operating margin.

Without the right insight, and relying on simple BER, you will miss significant issues with modern high-speed Ethernet ICs, modules and systems. Only a view which instantly highlights the impact of the error profile and gives insight into the ‘error fingerprint’ can help with PAM-4 based interfaces.

The VIAVI ONT family has all this integrated to help validate and debug PAM-4, and prevent you from being bamboozled by bit errors!



The [VIAVI ONT-800](#) provides deep measurements and instant insights

## VIAVI Can Help!

To get an insightful view of your high-speed optical module performance using testing solutions that meet the highest industry standards—[speak to our VIAVI applications team](#).

Also, please read our recent blogs:

[When 'Just Good Enough' isn't Good Enough](#)

[Integrated Testing Simplifies DCO Complexities](#)

[What's All the 800G Stuff? Evolution, Revolution...or Both?](#)

[What's All This Error Fingerprint Stuff?](#)

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Contact Us **+1 844 GO VIAVI**  
(+1 844 468 4284)

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